



# Accumulation-mode gate-all-around si nanowire nMOSFETs with sub-5 nm cross-section and high uniaxial tensile strain

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## ABSTRACT

In this work we report dense arrays of accumulation-mode gate-all-around Si nanowire nMOSFETs with sub-5 nm cross-sections in a highly doped regime. The integration of local stressor technologies (both local oxidation and metal-gate strain) to achieve  $\geq 2.5$  GPa uniaxial tensile stress in the Si nanowire is reported. The deeply scaled Si nanowire including such uniaxial tensile stress shows a low-field electron mobility of  $332 \text{ cm}^2/\text{V s}$  at room temperature, 32% higher than bulk mobility at the equivalent high channel doping. The conduction mechanism as well as high temperature performance was studied based on the electrical characteristics from room temperature up to  $\approx 400 \text{ K}$  and a  $V_{TH}$  drift of  $-1.72 \text{ mV/K}$  and an ionized impurity scattering-based mobility reduction were observed.

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## 1. Introduction

Lately, highly single-type doped Si devices such as accumulation-mode (AM) and junctionless (JL) MOSFETs are proposed as straightforward architectures to eliminate some technical limitations of the nano-scale MOSFETs such as ultra-abrupt junctions, allowing to fabricate even shorter channel devices [1–3]. Achieving a high driving current in heavily doped and especially in deeply scaled channels such as multi-gate nanowires and Fins is an engineering challenge due to the limitation of carrier mobility by ionized impurity scattering (see e.g. [4]) and the integration of mobility boosters such as local stressors in a CMOS process flow including suspended channels.

In this paper, we represent a fabrication process to make deeply scaled highly doped sub-5 nm Si nanowires from a top-down SOI platform and integrate it with the local stress platforms, local oxidation [5] and metal-gate strain [6], to include  $\geq 2.5$  GPa uniaxial tensile stress in the channel to boost the carrier mobility in highly doped AMOSFETs, without affecting the  $I_{ON}/I_{OFF}$  value.

## 2. Process flow to make dense array of accumulation-mode GAA suspended uniaxially tensile strained Si nanowire nMOSFETs

Fig. 1 represents the process flow. The fabrication process is started using 100 mm (100) Unibond SOI wafers (SOI/BOX = 340/400 nm) with intrinsic p-type doping and 525  $\mu\text{m}$  thickness. The SOI layer was thinned down to  $\approx 100 \text{ nm}$  by sacrificial dry oxida-

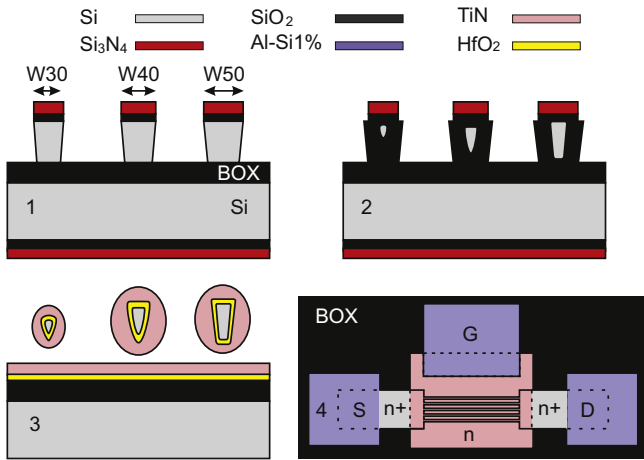
tion. The oxide layer was stripped by BHF and afterward, phosphorous ion implantation ( $20 \text{ keV}$ ,  $5 \times 10^{13} \text{ cm}^{-2}$ ) was done in the presence of a 20 nm thick LTO layer as the implantation mask on top of the SOI layer and followed by a 4 h furnace annealing at  $1000^\circ\text{C}$  to create a nominal  $1 \times 10^{18} \text{ cm}^{-3}$  n-type SOI layer. Afterward, a hard mask including 15 nm of  $\text{SiO}_2$  and 80 nm of LPCVD  $\text{Si}_3\text{N}_4$  was grown/deposited on the wafer and later on, dense arrays ( $\approx 8 \text{ nanowire}/\mu\text{m}$ ) of 10 parallel Si nanowires in  $\langle 110 \rangle$  as well as  $\langle 100 \rangle$  orientations, with 20–60 nm width and 0.5–3.0  $\mu\text{m}$  length, together with the S/D pad patterns were written using e-beam lithography (150 nm thick negative tone XR-1541-006 HSQ, exposure parameters in Vistec EBPG5000: 100 keV, 3000  $\mu\text{C}/\text{cm}^2$  dose).

The hard mask was etched using an anisotropic fluorine based dry etching and afterward, the SOI device layer was etched using a  $\text{HBr}/\text{O}_2$  based dry etching to create slanted Si side-walls to shrink the width further along the Fin to be able to deplete the highly doped channel properly (see Fig. 2). To reduce the Fin width even below 10 nm, round the sharp Si corners as well as accumulate uniaxial tensile stress in the suspended Si nanowire [5], a 7 h stress-limited dry oxidation at  $925^\circ\text{C}$  (0.500 L/min  $\text{O}_2$ , 10.00 L/min  $\text{N}_2$ ), to consume nominally 9 nm of (100) Si, in the presence of the tensile nitride hard mask was done. It is worth mentioning that the Si consumption on the slanted Si side-walls was observed to be  $\approx 40\%$  higher than (100) Si surface. As Figs. 1, 3 and 4 represent, Si nanowires with triangular as well as trapezoidal cross-sections can be achieved from this process flow depending on the initial width of the Fins before oxidation.

Hot phosphoric acid ( $155^\circ\text{C}$ ) was used to strip the nitride hard mask. Afterward, RCA (including 8 min HF dip to strip the grown  $\text{SiO}_2$  and suspend the Si nanowires from the substrate), 5 nm  $\text{HfO}_2$  deposition by ALD, RTA annealing ( $600^\circ\text{C}$ , 15 min) and

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**Fig. 1.** Process flow to make accumulation-mode GAA suspended uniaxially tensile strained Si nanowire nMOSFETs on a SOI substrate. W30 represents the initial 30 nm nanowire width on the mask.

finally, 50 nm TiN deposition by sputtering including intrinsic compressive thin film stress were done to make the gate stack as well as accumulate more uniaxial tensile stress in the suspended Si nanowires [6].

Gate patterning (including a 50/10 nm of LPCVD  $\text{Si}_3\text{N}_4/\text{LTO}$  mask, optical lithography and metal-gate/high- $k$  etching), S/D ion implantation by phosphorous and annealing ( $2 \times 10^{20} \text{ cm}^{-3}$  nominal doping), metallization (Al-Si1%) and finally, post-metallization annealing (450 °C, 30 min) were the further process steps.

### 3. Stress measurement method for the buckled gate-all-around Si nanowires

Fig. 3 represents the top-view SEM micrograph of an array of buckled Si nanowires right after the gate stack step, with the depicted TEM cross-sections. Using micro-Raman spectroscopy is pretty challenging to measure the stress value in the channel of such GAA Si nanowires with a high- $k$ /metal-gate stack due to the non-transparency of the metal-gate layer. Therefore, by assuming a Gaussian buckling profile along the Si nanowire and considering only the represented in-plane buckling in Fig. 3, the average uniaxial tensile stress/strain value is estimated to be  $\geq 2.5 \text{ GPa}/1.5\%$  (assuming Si Young's modulus of 169 GPa).

According to [7], the electron mobility enhancement is saturating in the Si-based MOSFETs by including  $>2.0 \text{ GPa}$  uniaxial tensile stress in the channel and therefore, the highest nominal electron mobility enhancement is already expected in such bended Si nanowires. A more in-depth stress study in [8] reveals that the uniaxial

tensile stress/strain level for similar  $2.0 \mu\text{m}$  long GAA Si nanowires can be up to  $5.6 \text{ GPa}/3.3\%$  considering both in-plane and out-of-plane buckling using both top and tilted-view SEM micrographs. According to [9] and as expected from the buckling profile in the SEM micrograph in Fig. 3, such strained Si nanowires are in the elastic regime and therefore, no carrier degradation is expected due to no plastic deformation in the channel.

## 4. Electrical characterization

### 4.1. Room temperature (298 K)

A setup including a Cascade prober and a HP 4155B Semiconductor Parameter Analyzer was used for electrical characterization at different temperatures. Figs. 5 and 6 represent the transfer, transconductance and output characteristic of a GAA AMOSFET including an array of 10 deeply scaled Si nanowires in  $\langle 110 \rangle$  orientation, depicted SEM and TEM micro/nanographs in Fig. 3, at 298 K. The  $\langle 110 \rangle$  orientated Si nanowire devices were chosen simply to investigate the highest uniaxial tensile stress-induced performance [7].

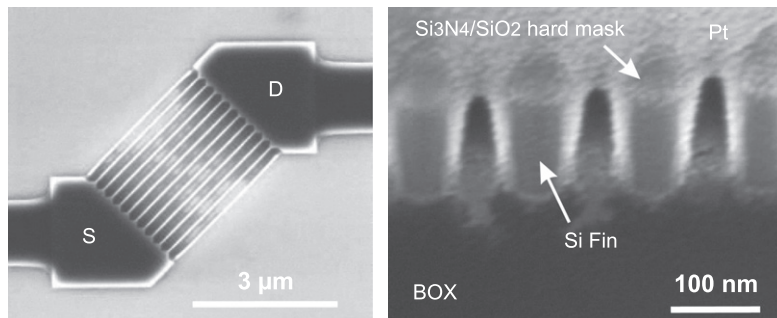
### 4.2. Demonstration of GAA deeply scaled Si nanowire as a high performance MOSFET

To investigate high temperature performance of GAA deeply scaled Si nanowire AMOSFETs, electrical characterization of the same device, depicted SEM and TEM micro/nanographs in Fig. 3, was done at 298–398 K with a 25 K step using the mentioned setup in Section 4.1 and the transfer characteristics were plotted in Fig. 7. Parallel to the high temperature performance MOSFET demonstration, this study will be used in Section 5.5 for further scattering mechanism detection in nanoscale.

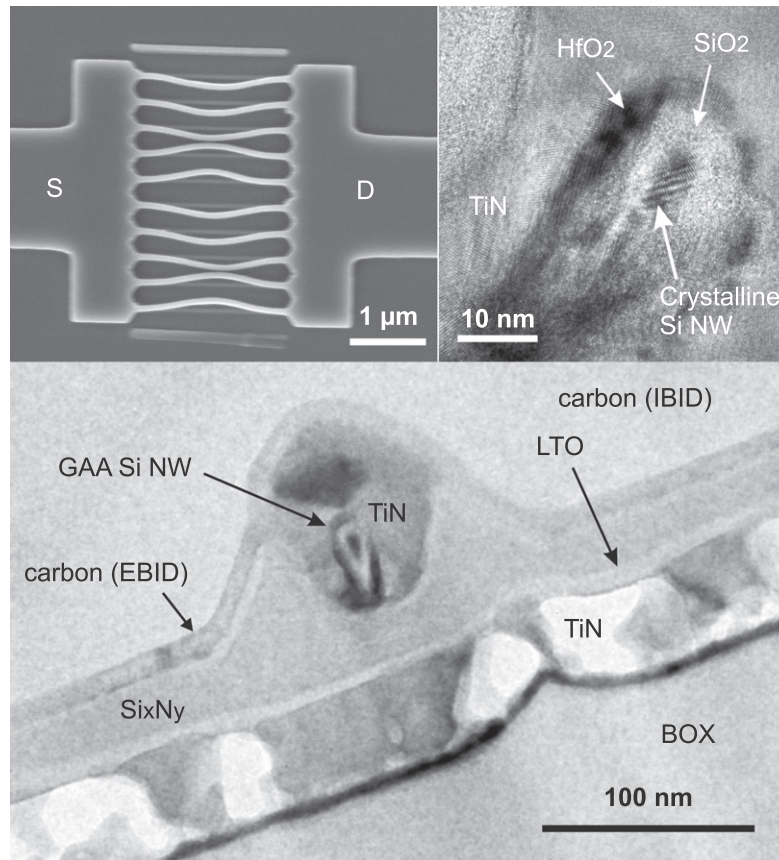
## 5. Extraction of parameters and discussion

### 5.1. Conduction mechanism in accumulation-mode and junctionless regimes

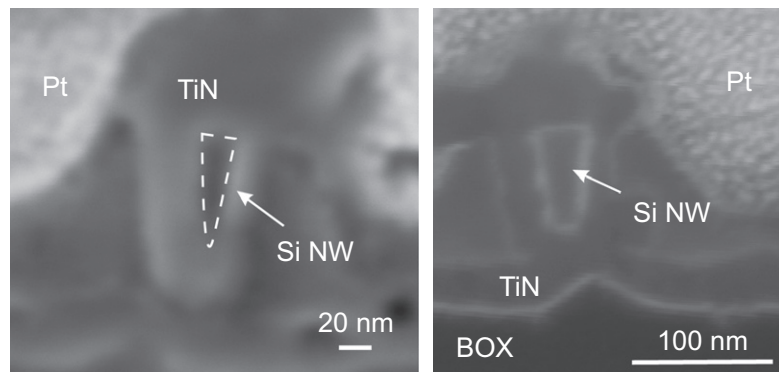
There is no junction in both AM and JL MOSFETs (a single type doping) while the doping level of the channel will nominally define the device type (heavily doped devices,  $>1 \times 10^{19} \text{ cm}^{-3}$ , called junctionless). The both devices have almost the same operation mechanism and the  $V_{FB}-V_{TH}$  difference can be engineered by doping level modulation in the channel. Therefore, the main operation regime for the heavily doped devices (JL) is usually bulk ( $V_{TH} < V_{GS} < V_{FB}$ ), due to the large  $V_{FB}-V_{TH}$  difference, and for slightly or highly doped devices (AM) is accumulation ( $V_{GS} > V_{FB}$ ). Operation in the bulk regime has the advantage of less degradation



**Fig. 2.** SEM micrograph of a HSQ pattern including  $3.0 \mu\text{m}$  long and  $25 \text{ nm}$  wide array of nanowires in  $\langle 100 \rangle$  orientation (left); SEM nanograph of Si Fins with  $\approx 88.6^\circ$  slanted side-walls, obtained using  $\text{HBr}/\text{O}_2$  chemistry (right).



**Fig. 3.** SEM micrograph of a buckled array of GAA Si nanowires after the gate stack step (left); TEM nanograph from the channel (right); TEM nanograph from the cross-section of a GAA Si nanowire (bottom). The cross-section of the Si nanowire is triangular with  $W_{top} \approx 4$  nm.



**Fig. 4.** SEM micrographs from the cross-section of the GAA triangular (W40) and trapezoidal (W50) Si nanowires, after the gate stack step.

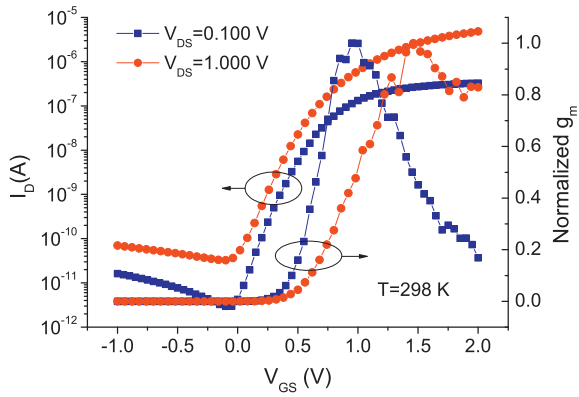
of carrier mobility due to the perpendicular field (conduction at the middle part of the channel) [10] but suffering from a non-straight forward analytical model in this region [11].

## 5.2. TCAD Sentaurus Device simulation of GAA deeply scaled Si nanowires

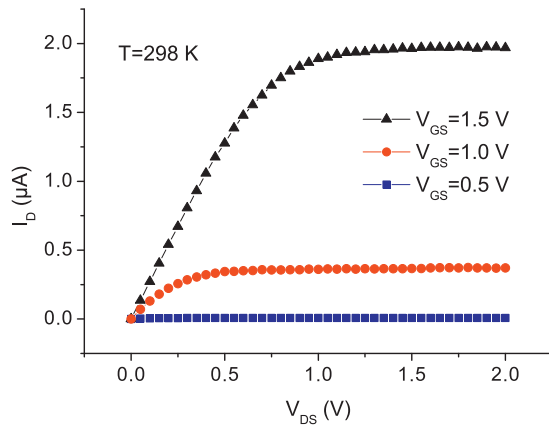
TCAD Sentaurus Device simulation (V. 2010.12) was used for 3D simulation of a GAA deeply scaled rounded triangular Si nanowire AMOSFET (see Fig. 8), with a similar cross-section depicted in the TEM nanograph in Fig. 3, similar channel and S/D doping but a shorter gate length (100 nm). The density-gradient model was used in the simulations to describe the 3D quantization effects in

such a deeply scaled Si nanowire with sub-5 nm cross-section. The transfer characteristics with and without quantum correction at  $V_{DS} = 100$  mV were plotted in Fig. 8. The threshold voltage for each case was extracted from the simulation data using the derivative of  $g_m/I_D$  method [12], minimizing the effect of gate-voltage dependent mobility and series-resistance. Quantum confinement was found to upshift the threshold voltage by 45 mV, a similar trend to the inversion-mode devices due to the higher quantized subband energies [13,14], and degrade the drain current, as shown in Fig. 8, from 8% in strong accumulation ( $V_{GS} = 1.300$  V) to 90% in the subthreshold region ( $V_{GS} = 0.200$  V).

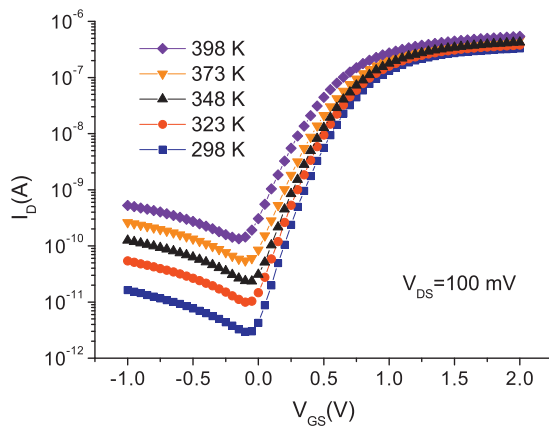
The flat-band voltage of the deeply scaled GAA Si nanowire AMOSFET was considered as a gate voltage that the electrostatic



**Fig. 5.** Transfer and transconductance characteristics of a GAA uniaxially tensile strained Si nanowire AMOSFET at 298 K. The  $g_m$  values were normalized to the  $g_m$  peaks ( $3.8 \times 10^{-7}$  and  $5.0 \times 10^{-6}$  S for  $V_{DS} = 0.100$  and  $1.000$  V, respectively).



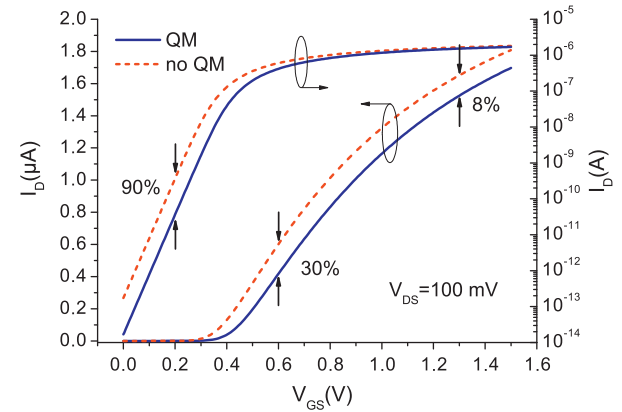
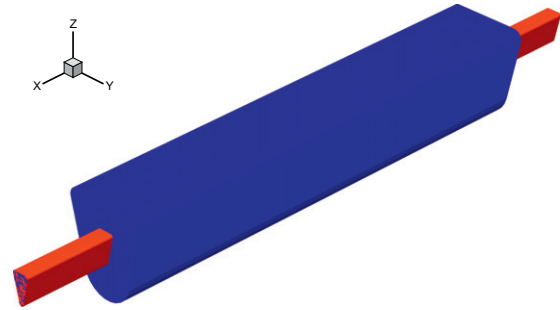
**Fig. 6.** Output characteristics of a GAA uniaxially tensile strained Si nanowire AMOSFET at 298 K.



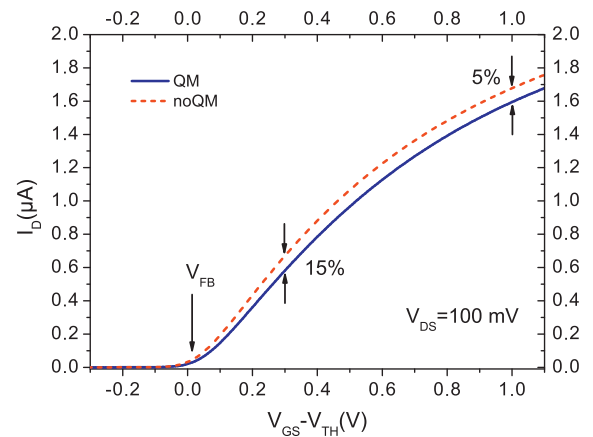
**Fig. 7.** Transfer characteristics of a GAA uniaxially tensile strained Si nanowire AMOSFET at different temperatures.

potential is almost constant across the channel cross-section (in both  $y$  and  $z$  directions) without considering any quantum mechanical effect, found to be  $0.342$  V ( $\approx 12$  mV above the threshold voltage).

To study better the effect of quantum confinement on only the current degradation, the drain currents are plotted vs. gate overdrive voltage ( $V_{GS} - V_{TH}$ ) in Fig. 9. The drain current was found to



**Fig. 8.** The 3D structure used for TCAD Sentaurus Device simulation (top) and the transfer characteristic results at  $V_{DS} = 100$  mV (bottom) with and without considering quantum mechanical effect ( $V_{TH}(\text{no QM}) = 0.330$  V,  $V_{TH}(\text{QM}) = 0.375$  V). The gate length is  $100$  nm.

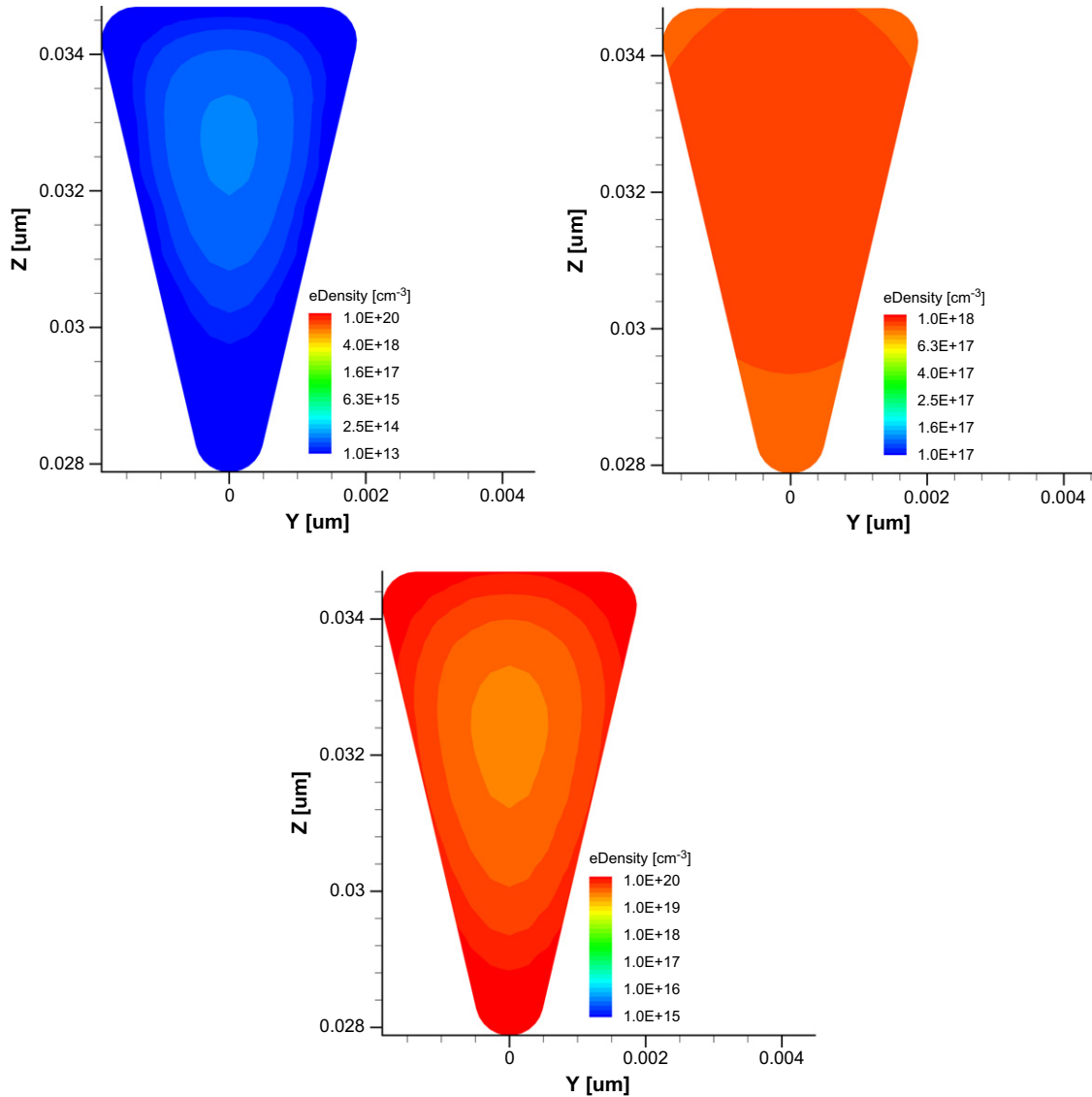


**Fig. 9.** Drain current vs. gate overdrive voltage ( $V_{GS} - V_{TH}$ ) with and without considering quantum mechanical effect.

drop from 15% to 5% by increasing the gate overdrive voltage from  $0.300$  to  $1.000$  V (see Fig. 9). Therefore, the quantum effect was found to be significant at the first glance combining both threshold voltage and drain current shifts in Fig. 8, but its effect on only the drain current degradation seems to be negligible in only strong accumulation regime leading to extract the key MOSFET parameters for a deeply scaled Si nanowire MOSFET, as a good approximation using the classical extraction methods in the strong accumulation regime.

To understand better the conduction mechanism in such a deeply scaled channel with corners, the electron densities at the





**Fig. 10.** The simulated electron density in the cross-section of a GAA deeply scaled Si nanowire AMOSFET in different regimes (cut at the middle of the device shown in Fig. 8, the surrounding gate dielectric is not shown): subthreshold (left,  $V_{GS} = 0.100$  V), between the threshold and the flat-band voltage (middle,  $V_{GS} = 0.340$  V), above the flat-band voltage and in the strong accumulation regime (right,  $V_{GS} = 1.500$  V). The simulations exclude any quantum correction.

middle of the device were plotted in Fig. 10 for three different gate voltages representing subthreshold, above the threshold and above the flat-band voltages. According to Fig. 10, bulk conduction is the main conduction mechanism below the flat-band voltage while in the strong accumulation regime, surface conduction as well as corner effect plays the major rule in the conduction mechanism. As shown in Fig. 11, the electron density distribution in the channel cross-section is mainly rearranged by quantum confinement in the strong accumulation regime.

### 5.3. Analytical model in the strong accumulation regime

At the first glance, the device represented in Fig. 3 can be seen as a degenerate double-gate architecture and therefore, an estimation of the accumulation current can be obtained from [11]. Indeed, noting that in the linear accumulation regime ( $V_{DS} < V_{GS} - V_{FB}$ ), the log terms can be discarded in the charge vs. potential and retaining only the highest order term in Eqs. (16), (22), and (24) in [11] (an assumption valid only in strong accumulation), we obtain (using source as a reference):

$$I_D(V_{GS}) = I_{Bulk} + I_{Acc}(V_{GS}) \quad (1)$$

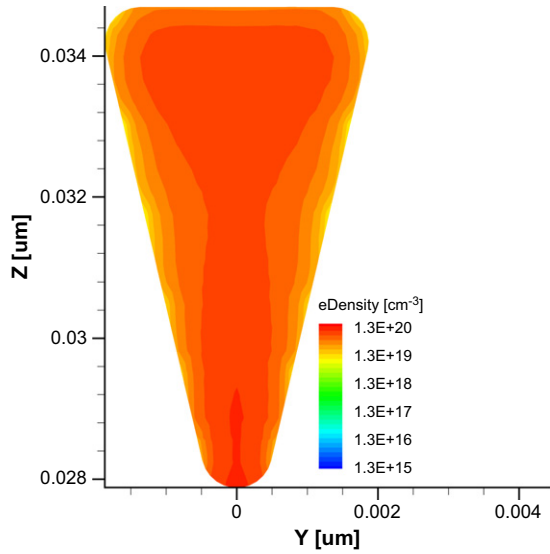
where  $I_{Bulk}$  does not increase further by  $V_{GS}$  and this fixed term in the strong accumulation regime represents the current carried out from a uniformly doped Si channel, ignoring the field effect. The accumulation current equals:

$$I_{Acc}(V_{GS}) = \mu \cdot C_{ox} \cdot W_{eff}/L \cdot \left[ (V_{GS} - V_{FB}) \cdot V_{DS} - 0.5 \cdot V_{DS}^2 \right] \quad (2)$$

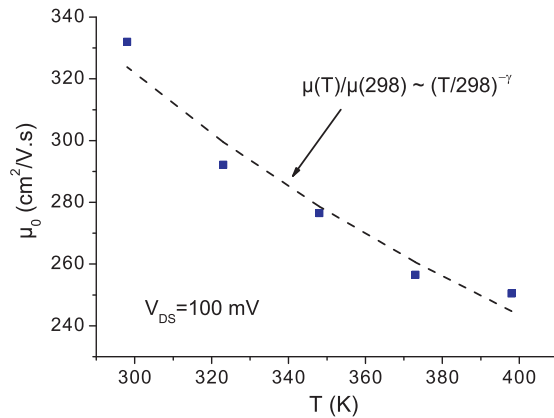
where  $\mu$ ,  $W_{eff}$ ,  $L$  and  $C_{ox}$  are mobility, effective channel width, channel length and gate oxide capacitance, respectively. Apart from these differences, such an asymptotic relationship derived for strong accumulation reverts to the one commonly used for bulk MOSFETs operating under high inversion. This property will serve as a basis to extract mobility related parameters considering  $W_{eff}$  as the channel electrical width.

### 5.4. Low-field electron mobility extraction in accumulation regime

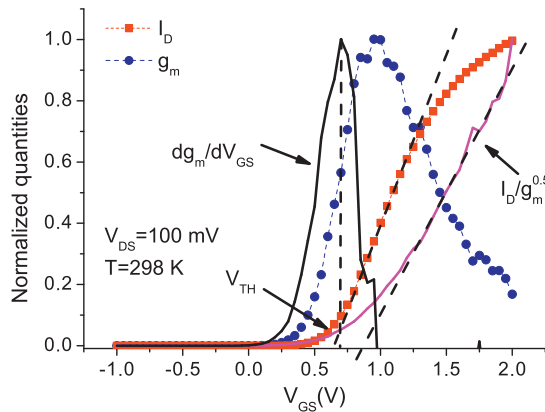
Since the bulk current does not change above  $V_{FB}$  and not contributing significantly in the conduction in that regime, low-field



**Fig. 11.** The simulated electron density in the cross-section of a GAA deeply scaled Si nanowire AMOSFET considering quantum correction (cut at the middle of the device, the surrounding gate dielectric is not shown), above the flat-band voltage and in the strong accumulation regime ( $V_{GS} = 1.500$  V). The electron density in the channel cross-section is rearranged by quantum confinement.

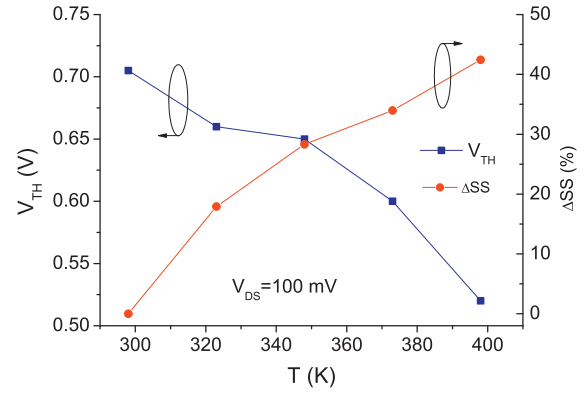


**Fig. 12.** Low-field electron mobility dependence on temperature for a GAA uniaxially tensile strained Si nanowire AMOSFET. The extracted  $\gamma$  is 0.966.



**Fig. 13.**  $V_{TH}$  and low-field electron mobility extraction of an AMOSFET using the transconductance change [24] and  $I_D/\sqrt{g_m}$  [15] methods.

electron mobility in the accumulation regime can be extracted simply using the  $I_D/\sqrt{g_m}$  method [15] in the strong accumulation



**Fig. 14.** Temperature dependence of threshold voltage and subthreshold slope of a GAA uniaxially tensile strained Si nanowire AMOSFET.

regime, independent of series resistance and mobility attenuation factor. To extract the low-field electron mobility, a cylindrical model, similar to [16], was used to expect the  $C_{ox}$  value for the GAA deeply scaled nanowires.

In this work, the extracted low-field electron mobility at  $V_{DS} = 100$  mV is  $332 \text{ cm}^2/\text{V.s}$ , 32% higher than bulk Si electron mobility at the same level of doping ( $1 \times 10^{18} \text{ cm}^{-3}$ ) [17], which is an evidence of including uniaxial tensile stress in the channel, and possibly a higher level can be achieved in this level of stress [7] in the case of an optimum dielectric-channel interface quality especially for the deeply scaled channels [18].

### 5.5. Scattering mechanism in deeply scaled highly doped Si nanowires

Fig. 12 depicts the low-field electron mobility at different temperatures for a single deeply scaled AMOSFET device. According to [19], the carrier mobility in the scattering regime ( $T > 100$  K) is varying by temperature according to the following trend:

$$\mu(T)/\mu(T_0) = (T/T_0)^{-\gamma} \quad (3)$$

where  $T_0 = 298$  K. According to Fig. 12,  $\gamma = 0.966$  which is quite lower than 2.5, reported for the GAA Si nanowire MOSFETs with intrinsic doping level [20]. Our experiment in [21] is also reporting a similar  $\gamma$  value for the GAA triangular Si nanowires with a slightly bigger cross-section (sub-20 nm) with the same doping level. All the three studies in [20–22] are in line with the previous reports for intrinsic or low-doped Si [23] being explained by the dominant role of ionized impurity scattering in highly doped Si MOSFETs, even for the deeply scaled Si nanowires.

### 5.6. Threshold voltage extraction

The threshold voltage of a MOSFET, in general, can be extracted using the transconductance change (TC) method [24], quasi-independent of series resistance and no need to any accurate analytical model. Interestingly, as shown in Fig. 13, the TC peak is located almost at the expected (theoretical) threshold voltage from the linear part of the transfer characteristic. It is worth mentioning that the derivative of  $g_m/I_D$  method to extract the threshold voltage [12], used in Section 5.2 for the simulation data could not provide consistent results using the measurement data. Fig. 14 represents a  $V_{TH}$  drift of  $-1.72 \text{ mV/K}$  (smaller than  $-2.1 \text{ mV/K}$ , the prior reported value for a deeply scaled GAA low doped Si nanowire in [20]) and a subthreshold slope change of  $0.404\%/K$  (with subthreshold slope of  $106 \text{ mV/dec.}$  at room temperature) for the 298–398 K temperature range.

Since the accumulation-mode and junctionless transistors work in a simple MOSFET-like manner only above the flat-band voltage but not above the threshold voltage [11], direct extraction of the flat-band voltage as a key MOSFET parameter from the characterization data seem to be pretty necessary. At the first glance, the  $V_{FB}$  value is expected to be extracted using the intersect of the two quasi-straight lines above the threshold voltage corresponding to the bulk and accumulation regimes in the transfer characteristic [25] or using  $I_D/\sqrt{g_m}$  in the strong accumulation regime as an approximation [21,22]. TCAD Sentaurus Device simulation reveals that the  $V_{FB}-V_{TH}$  difference for the deeply scaled cross-section in Fig. 5 is  $\approx 12$  mV at  $1 \times 10^{18} \text{ cm}^{-3}$  phosphorous doping level and at 298 K. Therefore, the direct  $V_{FB}$  extraction from e.g. the transfer characteristic of our deeply scaled Si nanowire MOSFETs is almost beyond the accuracy of the extraction methods and the  $V_{FB}$  value simply should be approximated using the TCAD simulations at various temperatures. It is also worth mentioning that the both mentioned  $V_{FB}$  extraction methods seem to be pretty sensitive to the series resistance for the multi-gate scaled devices (see [26,12]) and several efforts should be addressed to the extraction methods for such multi-gate scaled devices.

## 6. Conclusion

We demonstrated dense array of accumulation-mode gate-all-around deeply scaled top-down Si nanowire nMOSFET with cross-section smaller than 5 nm on a SOI substrate with an electron mobility boost due to  $\geq 2.5$  GPa uniaxial tensile stress in the channel. The GAA deeply scaled Si nanowires were demonstrated as high temperature performance MOSFETs in a temperature range from 298 K to 398 K. Finally, the scattering mechanism was studied in deeply scaled Si nanowires and in a highly doped regime and an ionized impurity based scattering was observed.

## Acknowledgements

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